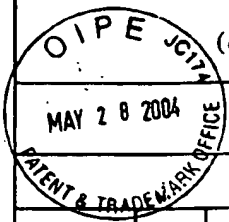
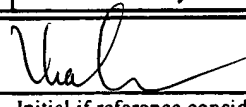




**315125.1**

5/28/04

<b>LIST OF REFERENCES CITED BY APPLICANT</b> <b>Form PTO-1449</b> (Use several sheets if necessary)					ATTY. DOCKET NO.: <b>4717-7500</b>		APPLICATION NO.: <b>10/615,259</b>				
<div style="display: inline-block; vertical-align: middle;">  </div> <div style="display: inline-block; vertical-align: middle; margin-left: 20px;"> Sheet 1 of 1 </div>					APPLICANT: <b>Bruno GHYSELEN et al.</b>			FILING DATE: <b>July 9, 2003</b>		GROUP: <b>2812</b>	
					<b>U.S. PATENT DOCUMENTS</b>						
*EXAMINER INITIAL	CITE NO.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE				
R	A1	6,524,935	02/2003	Canaperi et al	438	478	/				
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	A3	6,603,156	09/2003	Rim	257	190					
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<b>FOREIGN PATENT DOCUMENTS</b>											
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							YES	NO			
R	B1	2001168342	6/2001	JP			/				
	B2	WO 02/15244	02/2002	WO							
	B3	WO 02/27783	04/2002	WO							
	B4	WO 02/071493	09/2002	WO							
↓	B5	WO 02/080241	10/2002	WO							
<b>OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)</b>											
R	C1	Hobart, K.D. et al., <i>On Scaling the Thin Film Si Thickness of SOI Substrates, A Perspective on Wafer Bonding for Thin Film Devices</i> , Naval Research Laboratory, Electronics Science and Technology division Washington, DC 20375									
R	C2	Mizuno, T. et al., <i>High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMO Technology</i> , Electron Devices Meeting , 1999. IEDM Technical Digest International, Washington, DC, USA 5-8 December 1999, Piscataway, NJ									
R	C3	Tong, Q.Y. et al., <i>Semiconductor on Wafer Bonding</i> , Science and Technology, Interscience Technology, Johnson Wiley & Sons, Inc.									
EXAMINER				DATE CONSIDERED							
				8/20/04							
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.											